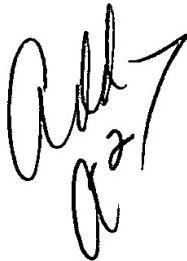


Abstract of the Disclosure:

A method and a circuit arrangement for protecting integrated circuits against electrostatic discharge (ESD) during and after packaging. An electrical connection between two

5 integrated circuits is made by producing a low-impedance connection in the first integrated circuit, between a signal pad and a pad for a supply potential. The connection has a portion of reduced cross section, which is preferably severed by a current pulse applied after the arrangement has been
10 assembled in a package and the connection has been electrically bonded to the second integrated circuit. The ESD protection during assembly requires no additional chip surface area.

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MPW/tg